1. An apparatus comprising:

a first transistor having a gate terminal, a drain terminal, and a source terminal;

a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor;

a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said second transistor is electrically connected to said source terminal of said first transistor; and,

a second resistor having a first and a second terminal, wherein said first terminal of said second resistor is electrically connected to said gate terminal of said second transistor, and wherein said second terminal of said second resistor is electrically connected to said drain terminal of said first transistor.

2. The apparatus of claim 1 wherein a first voltage connected to said second terminal of said second resistor is greater than a second voltage connected to said drain terminal of said second transistor by at least the gate-to-source threshold voltage of said second transistor.

3. The apparatus of claim 1 wherein said first transistor further comprises a first substrate terminal and said second transistor further comprises a second substrate terminal wherein said first substrate terminal and said second substrate terminal are electrically connected to each other.

4. The apparatus of claim 3 wherein said first substrate is connected to a ground voltage.

5. The apparatus of claim 3 further comprising:

a third resistor having a first and second terminals, wherein said first terminal of said third resistor is electrically connected to said source terminal of said first transistor and said second terminal of said third resistor is electrically connected to said substrate of said first transistor;

a third transistor having a gate terminal, drain terminal, source terminal, and substrate terminal, wherein said drain terminal of said third transistor is electrically connected to said gate terminal of said first transistor, and wherein said substrate terminal of said third transistor is electrically connected to said source terminal of said third transistor and to said substrate terminal of said first transistor.

6. The apparatus of claim 5 wherein said first transistor, said second transistor, and said third transistor are n-type depletion mode field effect transistors.

7. An apparatus comprising:

a first transistor having a gate terminal, a drain terminal, and source terminal;

a second transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said first transistor is electrically connected to said drain terminal of said second transistor;

a first resistor having a first terminal and second terminal, wherein said first terminal of said first resistor is electrically connected to said gate terminal of said first transistor; and,

a second resistor having a first terminal and second terminal, wherein said first terminal of said second resistor is electrically connected to said drain terminal of said second transistor, and wherein said second terminal of said second resistor is electrically connected to said gate terminal of said second transistor.

8. The apparatus of claim 7 further comprising:

a third transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said third transistor is electrically connected to said source terminal of said second transistor, and wherein said drain terminal of said third transistor is electrically connected to said first terminal of said second resistor;

a fourth transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said fourth transistor is electrically connected to said drain terminal of said third transistor, and wherein said drain terminal of said fourth transistor is electrically connected to said drain terminal of said first transistor; and,

a third resistor having a first terminal and second terminal, wherein said first terminal of said third resistor is electrically connected to said gate terminal of said fourth transistor, and wherein said second terminal of said third resistor is electrically connected to said second terminal of said first resistor.

9. The apparatus of claim 8 wherein a first voltage connected to said second terminal of said first resistor is greater than a second voltage connected to said drain terminal of said first transistor by at least the gate-to-source threshold voltage of said first transistor.

10. The apparatus of claim 8:

wherein said first transistor further comprises a substrate terminal,

wherein said second transistor further comprises a substrate terminal,

wherein said third transistor further comprises a substrate terminal, and

wherein said fourth transistor further comprises a substrate terminal,

wherein said substrate terminal of said first transistor is electrically connected to said source terminal of said second transistor,

wherein said substrate terminal of said second transistor is electrically connected to said source terminal of said second transistor,

wherein said substrate terminal of said third transistor is electrically connected to said source terminal of said third transistor, and

wherein said substrate terminal of said fourth transistor is electrically connected to said source terminal of said third transistor.

11. The apparatus of claim 10 wherein said first substrate is connected to a ground voltage.

12. The apparatus of claim 10 further comprising

a fifth transistor having a gate terminal, a drain terminal, a source terminal, and a substrate terminal, wherein said drain terminal of said fifth transistor is electrically connected to said gate terminal of said third transistor, and wherein said substrate terminal of said fifth transistor is electrically connected to said source terminal of said fourth transistor;

a sixth transistor having a gate terminal, a drain terminal, a source terminal, and a substrate terminal, wherein said drain terminal of said sixth transistor is electrically connected to said drain terminal of said fourth transistor, wherein said source terminal of said sixth transistor is electrically connected to said drain terminal of said fifth transistor, and wherein said substrate terminal of said sixth transistor is electrically connected to said source terminal of said fifth transistor; and

a fourth resistor having a first terminal and a second terminal, wherein said first terminal of said fourth resistor is electrically connected to said gate terminal of said sixth transistor, and wherein said second terminal of said fourth resistor is electrically connected to said second terminal of said first resistor.

13. The apparatus of claim 12 further comprising

a seventh transistor having a gate terminal, a drain terminal, a source terminal, and a substrate terminal, wherein said source terminal of said seventh transistor is electrically connected to said source terminal of said second transistor, wherein said gate terminal of

said seventh transistor is electrically connected to said drain terminal of said second transistor, and wherein said substrate terminal of said seventh transistor is electrically connected to said source terminal of said seventh transistor; and

a fifth resistor having a first terminal and second terminal, wherein said first terminal of said fifth resistor is electrically connected to said drain terminal of said seventh transistor, and wherein said second terminal of said fifth resistor is electrically connected to said drain terminal of said fourth transistor.

14. The apparatus of claim 13 wherein said first transistor, said second transistor, said third transistor, said fourth transistor, said fifth transistor, said sixth transistor, and said seventh transistor are n-type depletion mode field effect transistors.

15. The apparatus of claim 14 wherein said source terminal of said second transistor is connected to a ground voltage.